

**DRAM MODULE**

**KMM5328000CK/CKG & KMM5328100CK/CKG with Fast Page Mode**

8M x 32 DRAM SIMM using 4Mx4, 4K/2K Refresh, 5V

**GENERAL DESCRIPTION**

The Samsung KMM53280(1)00CK is a 8Mx32bits Dynamic RAM high density memory module. The Samsung KMM53280(1)00CK consists of sixteen CMOS 4Mx4bits DRAMs in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53280(1)00CK is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

**PERFORMANCE RANGE**

Speed	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>
-5	50ns	13ns	90ns
-6	60ns	15ns	110ns

**FEATURES**

- Part Identification
  - KMM5328000CK(4096 cycles/64ms Ref, SOJ, Solder)
  - KMM5328000CKG(4096 cycles/64ms Ref, SOJ, Gold)
  - KMM5328100CK(2048 cycles/32ms Ref, SOJ, Solder)
  - KMM5328100CKG(2048 cycles/32ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDPin & pinout
- PCB : Height(1000mil), double sided component

**PIN CONFIGURATIONS**

Pin	Symbol	Pin	Symbol
1	V <sub>ss</sub>	37	NC
2	DQ0	38	NC
3	DQ16	39	V <sub>ss</sub>
4	DQ1	40	$\overline{\text{CAS0}}$
5	DQ17	41	$\overline{\text{CAS2}}$
6	DQ2	42	$\overline{\text{CAS3}}$
7	DQ18	43	$\overline{\text{CAS1}}$
8	DQ3	44	$\overline{\text{RAS0}}$
9	DQ19	45	$\overline{\text{RAS1}}$
10	V <sub>cc</sub>	46	NC
11	NC	47	W
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	V <sub>cc</sub>
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	A11	65	DQ15
30	V <sub>cc</sub>	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{\text{RAS1}}$	69	PD3
34	$\overline{\text{RAS0}}$	70	PD4
35	NC	71	NC
36	NC	72	V <sub>ss</sub>

**PIN NAMES**

Pin Name	Function
A0 - A11	Address Inputs(4K Ref)
A0 - A10	Address Inputs(2K Ref)
DQ0 - DQ31	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS0}}$ , $\overline{\text{RAS1}}$	Row Address Strobe
$\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$	Column Address Strobe
PD1 -PD4	Presence Detect
V <sub>cc</sub>	Power(+5V)
V <sub>ss</sub>	Ground
NC	No Connection

**PRESENCE DETECT PINS (Optional)**

Pin	50NS	60NS
PD1	NC	NC
PD2	V <sub>ss</sub>	V <sub>ss</sub>
PD3	V <sub>ss</sub>	NC
PD4	V <sub>ss</sub>	NC

\* Pin connection changing available

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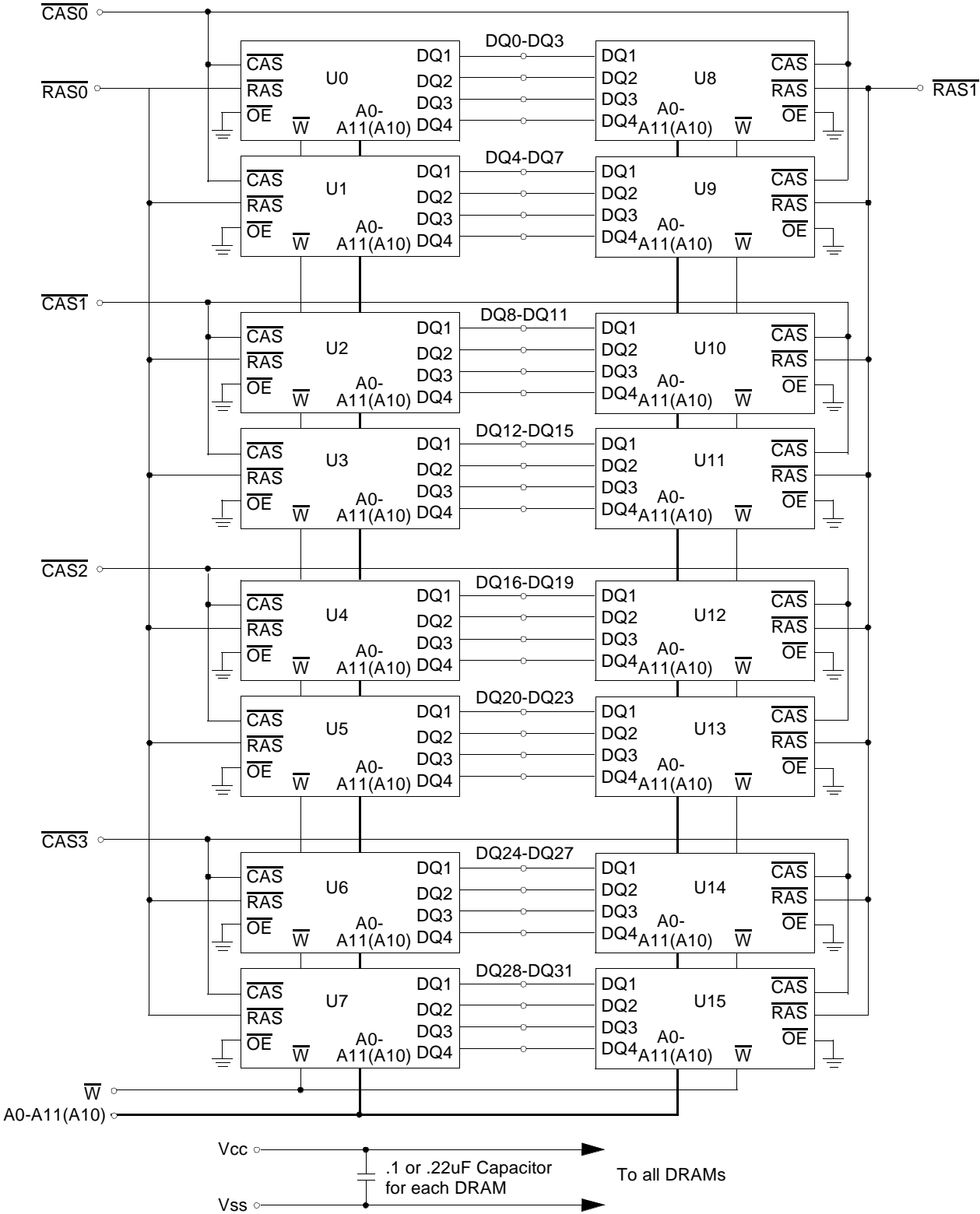
\* NOTE : A11 is used for only KMM5328000CK/CKG (4K ref.)



ELECTRONICS

**DRAM MODULE**

**FUNCTIONAL BLOCK DIAGRAM**



**DRAM MODULE**

**ABSOLUTE MAXIMUM RATINGS \***

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-1 to +7.0	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Power Dissipation	P <sub>d</sub>	16	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to V<sub>SS</sub>, T<sub>A</sub> = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	-	V <sub>CC</sub> +1 <sup>*1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-1.0 <sup>*2</sup>	-	0.8	V

\*1 : V<sub>CC</sub>+2.0V/20ns, Pulse width is measured at V<sub>CC</sub>.

\*2 : -2.0V/20ns, Pulse width is measured at V<sub>SS</sub>.

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5328000CK/CKG		KMM5328100CK/CKG		Unit
		Min	Max	Min	Max	
I <sub>CC1</sub>	-5	-	736	-	896	mA
	-6	-	656	-	816	mA
I <sub>CC2</sub>	Don't care	-	32	-	32	mA
I <sub>CC3</sub>	-5	-	736	-	896	mA
	-6	-	656	-	816	mA
I <sub>CC4</sub>	-5	-	656	-	736	mA
	-6	-	576	-	656	mA
I <sub>CC5</sub>	Don't care	-	16	-	16	mA
I <sub>CC6</sub>	-5	-	736	-	896	mA
	-6	-	656	-	816	mA
I <sub>I(L)</sub>	Don't care	-80	80	-80	80	uA
I <sub>O(L)</sub>	Don't care	-10	10	-10	10	uA
V <sub>OH</sub>	Don't care	2.4	-	2.4	-	V
V <sub>OL</sub>	Don't care	-	0.4	-	0.4	V

I<sub>CC1</sub> : Operating Current \* ( $\overline{RAS}$ ,  $\overline{CAS}$ , Address cycling @trc=min)

I<sub>CC2</sub> : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$ )

I<sub>CC3</sub> :  $\overline{RAS}$  Only Refresh Current \* ( $\overline{CAS}=V_{IH}$ ,  $\overline{RAS}$  cycling @trc=min)

I<sub>CC4</sub> : Fast Page Mode Current \* ( $\overline{RAS}=V_{IL}$ ,  $\overline{CAS}$  Address cycling : tPC=min)

I<sub>CC5</sub> : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$ )

I<sub>CC6</sub> :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current \* ( $\overline{RAS}$  and  $\overline{CAS}$  cycling @trc=min)

I<sub>I(L)</sub> : Input Leakage Current (Any input 0≤V<sub>IN</sub>≤V<sub>CC</sub>+0.5V, all other pins not under test=0 V)

I<sub>O(L)</sub> : Output Leakage Current(Data Out is disabled, 0V≤V<sub>OUT</sub>≤V<sub>CC</sub>)

V<sub>OH</sub> : Output High Voltage Level (I<sub>OH</sub> = -5mA)

V<sub>OL</sub> : Output Low Voltage Level (I<sub>OL</sub> = 4.2mA)

\* **NOTE** : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub> and I<sub>CC3</sub>, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In I<sub>CC4</sub>, address can be changed maximum once within one page mode cycle, tPC.



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**CAPACITANCE** ( $T_A = 25 \pm 1^\circ\text{C}$ ,  $V_{CC}=5\text{V}$ ,  $f = 1\text{MHz}$ )

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	CIN1	-	100	pF
Input capacitance[ $\overline{V}$ ]	CIN2	-	130	pF
Input capacitance[ $\overline{\text{RAS0}}$ , $\overline{\text{RAS1}}$ ]	CIN3	-	70	pF
Input capacitance[ $\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$ ]	CIN4	-	30	pF
Input/Output capacitance[ $\overline{\text{DQ0-31}}$ ]	CDQ	-	20	pF

**AC CHARACTERISTICS** ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ,  $V_{CC}=5.0\text{V} \pm 10\%$ . See notes 1,2.)

Test condition :  $V_{ih}/V_{il}=2.4/0.8\text{V}$ ,  $V_{oh}/V_{ol}=2.4/0.4\text{V}$ , Output loading  $CL=100\text{pF}$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4
Access time from $\overline{\text{CAS}}$	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	ns	6
Transition time(rise and fall)	tT	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	8
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		ns	
Data-in set-up time	tDS	0		0		ns	9
Data-in hold time	tDH	10		15		ns	9
Refresh period (4K Ref)	tREF		64		64	ms	
Refresh period (2K Ref)	tREF		32		32	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{\text{CAS}}$ setup time( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		ns	
$\overline{\text{CAS}}$ hold time( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	tRPC	5		5		ns	

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**AC CHARACTERISTICS** ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ . See notes 1,2.)

Test condition :  $V_{ih}/V_{il} = 2.4/0.8\text{V}$ ,  $V_{oh}/V_{ol} = 2.4/0.4\text{V}$ , Output loading  $C_L = 100\text{pF}$

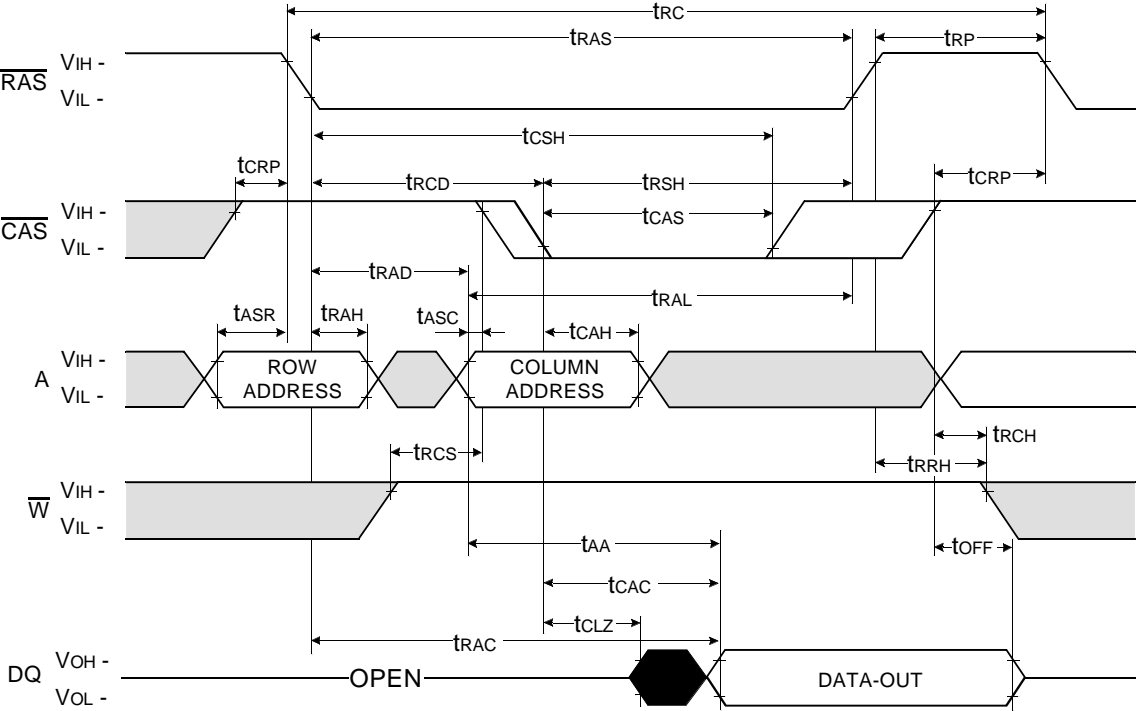
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35	ns	3
Fast page mode cycle time	tPC	35		40		ns	
$\overline{\text{CAS}}$ precharge time(Fast page cycle)	tCP	10		10		ns	
$\overline{\text{RAS}}$ pulse width(Fast page cycle)	tRASP	50	200K	60	200K	ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time(C-B-R refresh)	tWRP	10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time(C-B-R refresh)	tWRH	10		10		ns	
$\overline{\text{CAS}}$ precharge(C-B-R counter test)	tCPT	20		20		ns	

**NOTES**

1. An initial pause of 200us is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
2.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met.  $t_{RCD}(\text{max})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
5. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$ .
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
7.  $t_{WCS}$  is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
9. These parameter are referenced to the  $\overline{\text{CAS}}$  leading edge in early write cycles.
10. Operation within the  $t_{RAD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met.  $t_{RAD}(\text{max})$  is specified as reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled by  $t_{AA}$ .

DRAM MODULE

READ CYCLE

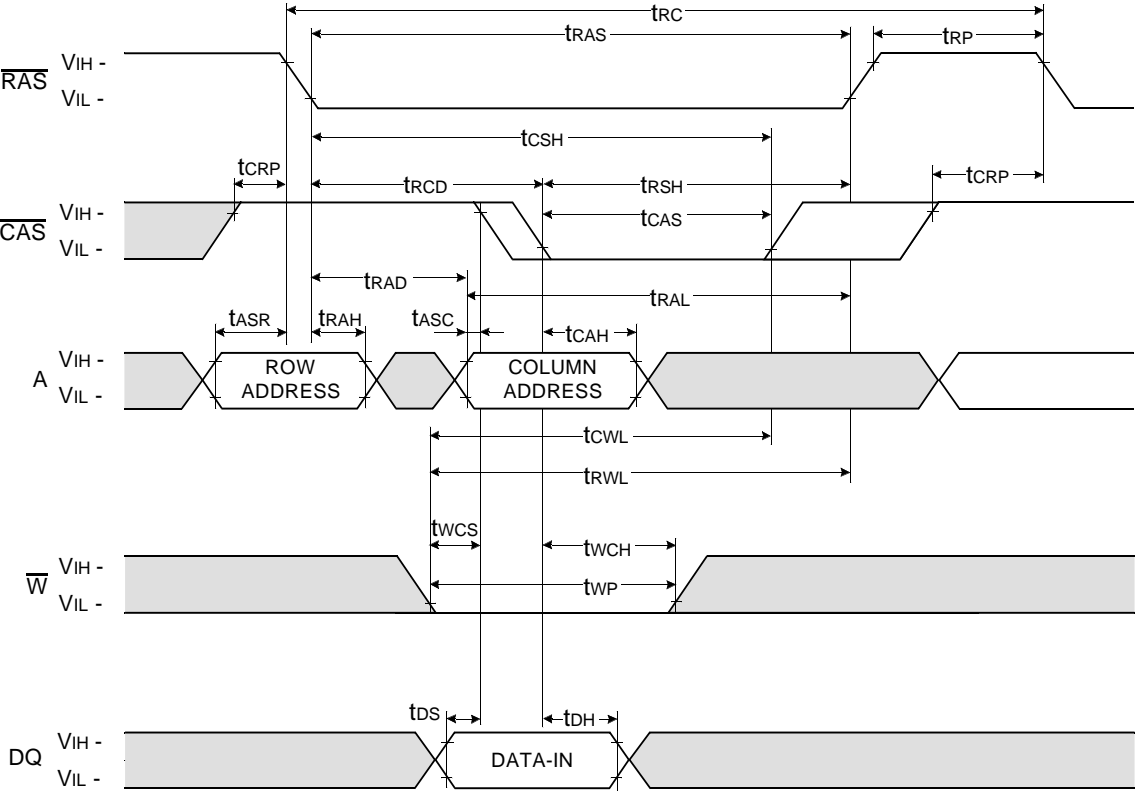


Don't care  
Undefined

DRAM MODULE

WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN

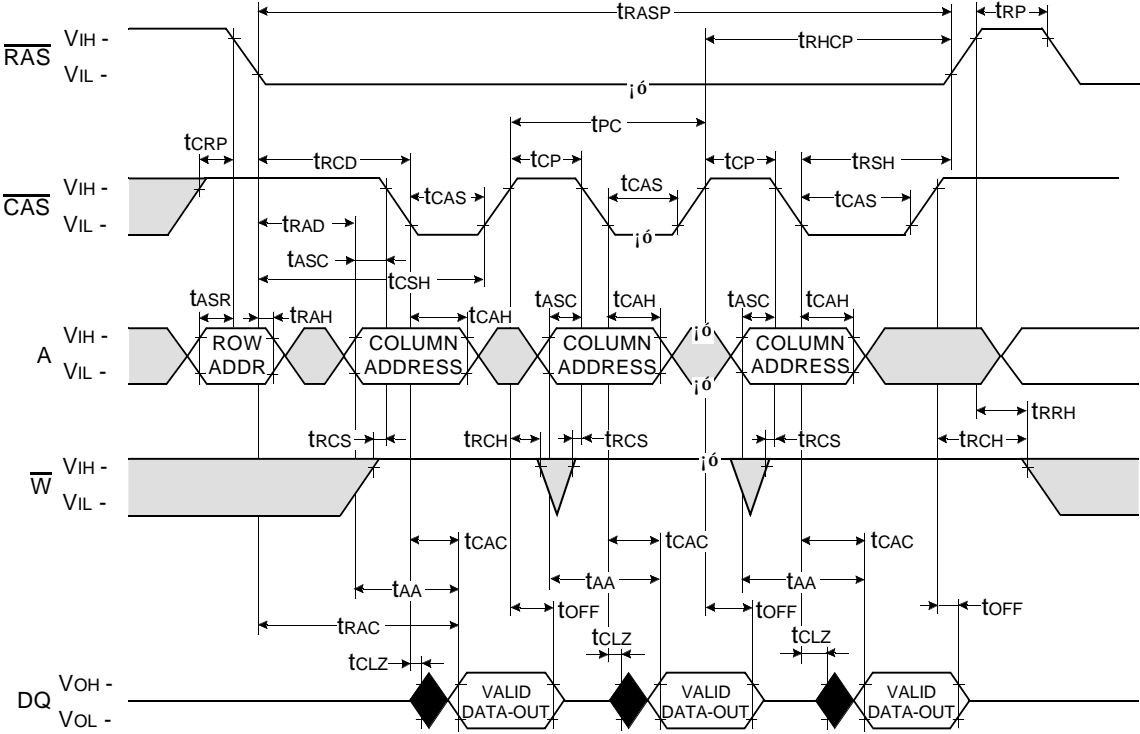




□ Don't care  
■ Undefined

**DRAM MODULE**

**FAST PAGE READ CYCLE**

NOTE : DOUT = OPEN



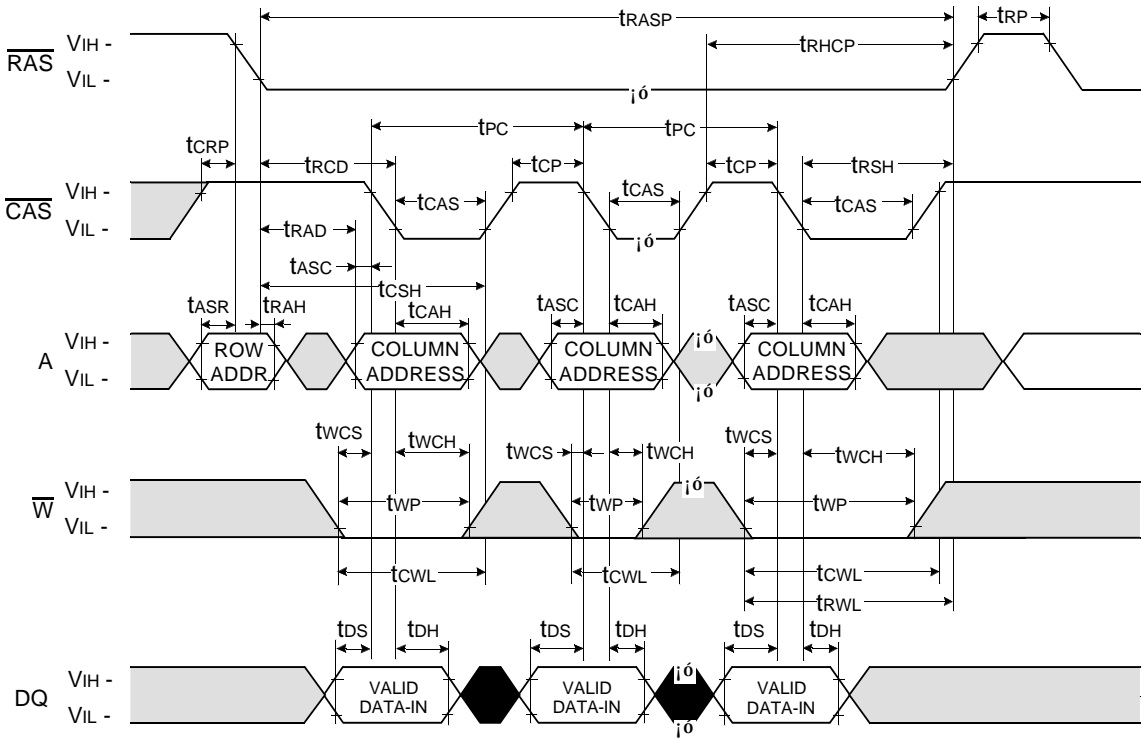
-  Don't care
-  Undefined



DRAM MODULE

FAST PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



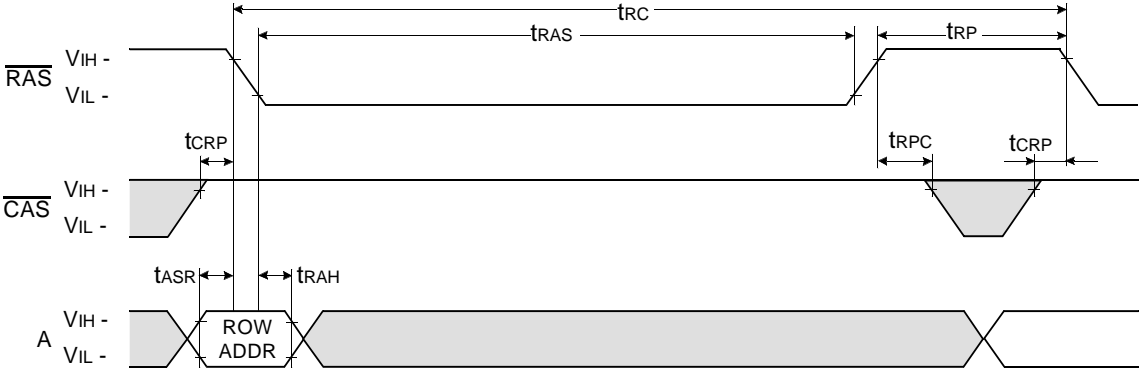
Don't care  
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DRAM MODULE

**RAS - ONLY REFRESH CYCLE**

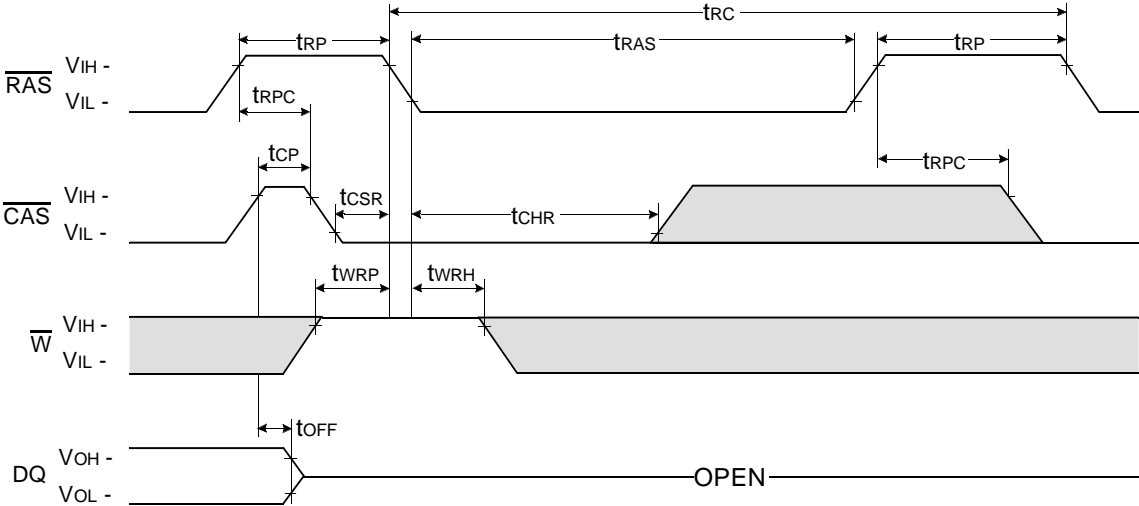
NOTE :  $\overline{W}$ ,  $\overline{OE}$ , DIN = Don't care

DOUT = OPEN



**CAS - BEFORE - RAS REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care

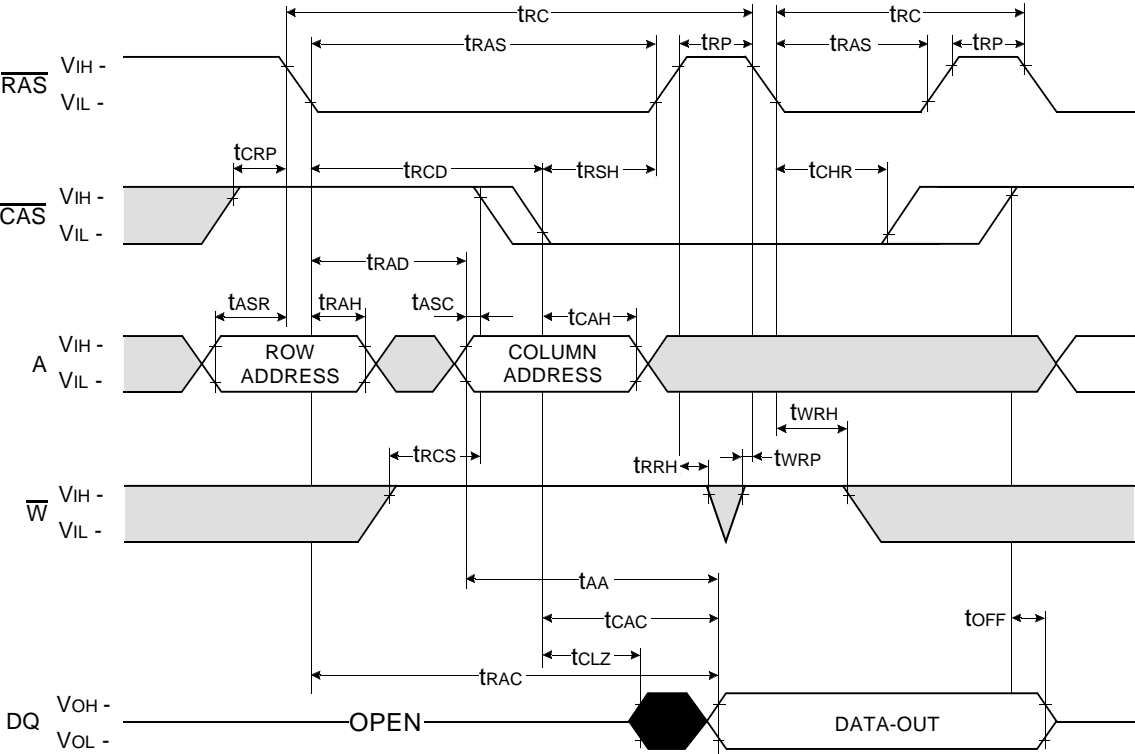


□ Don't care  
■ Undefined



DRAM MODULE

HIDDEN REFRESH CYCLE ( READ )

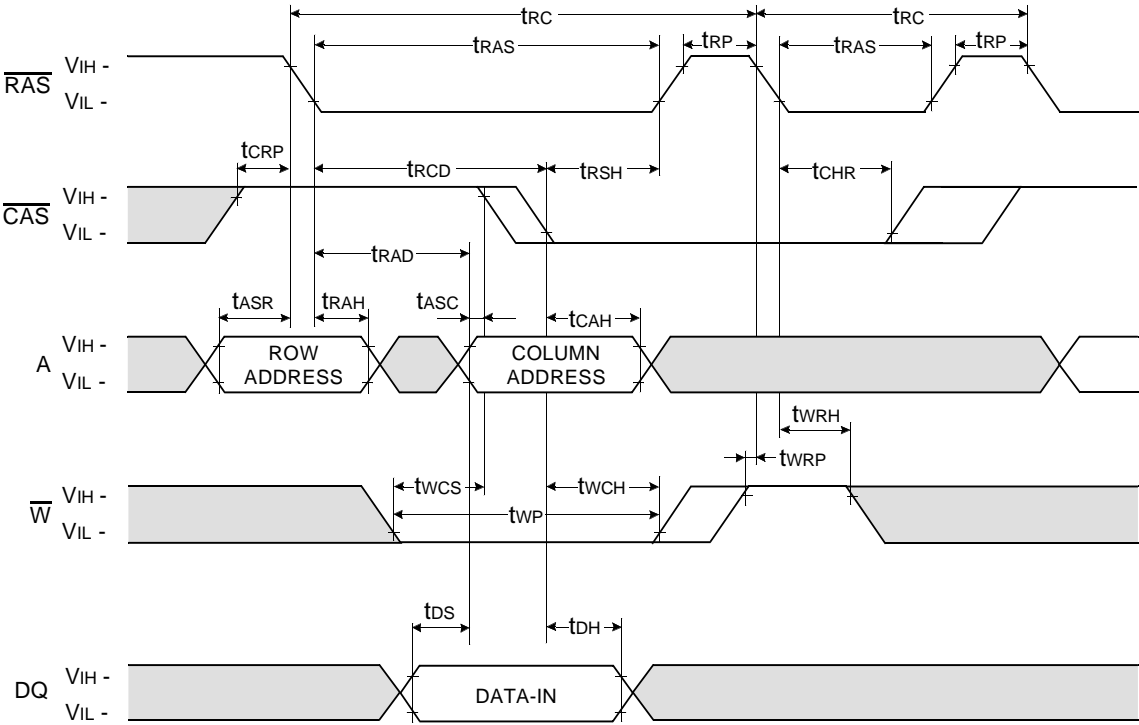


□ Don't care  
■ Undefined

DRAM MODULE

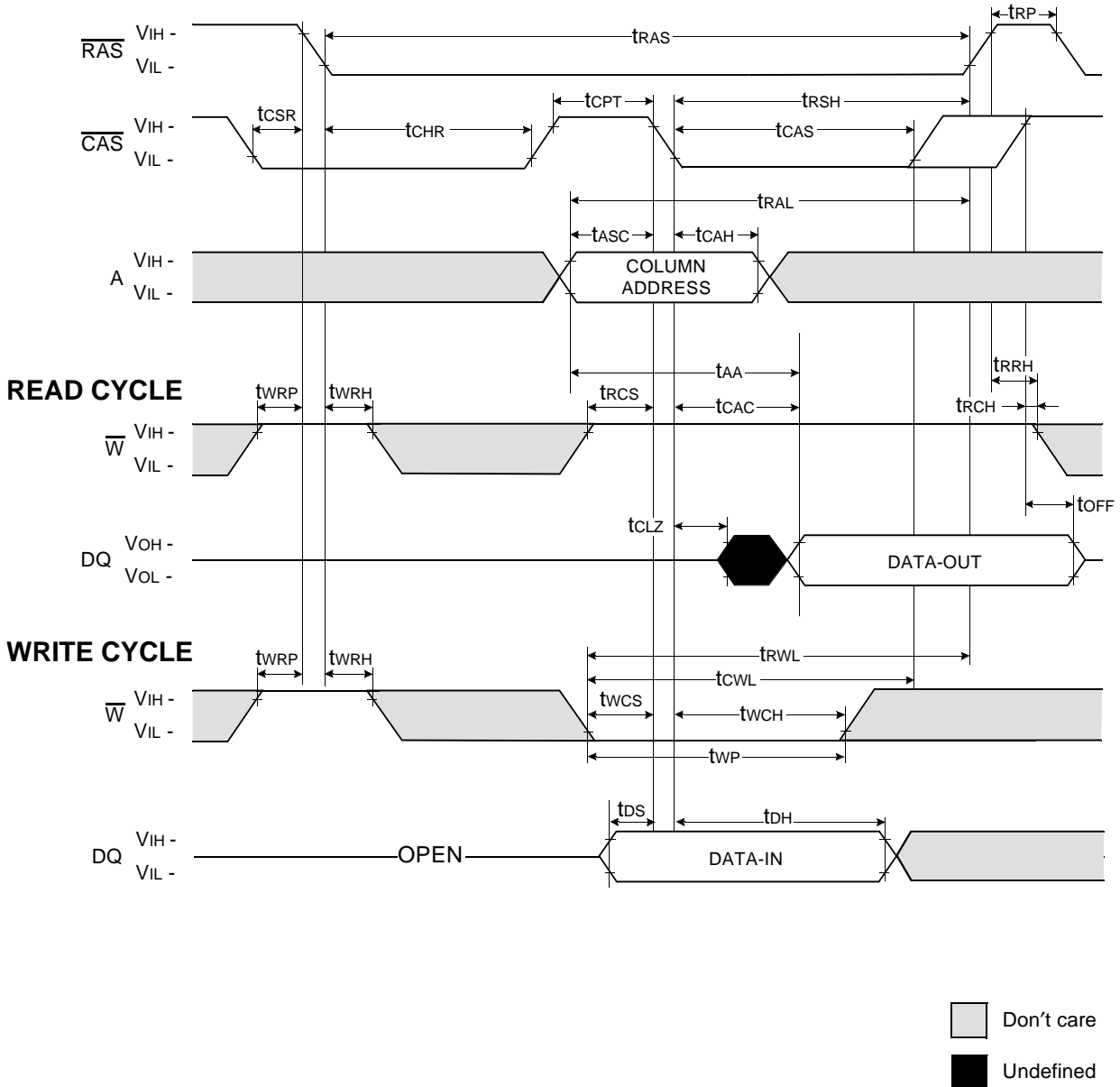
HIDDEN REFRESH CYCLE ( WRITE )

NOTE : DOUT = OPEN



□ Don't care  
■ Undefined

**CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE**

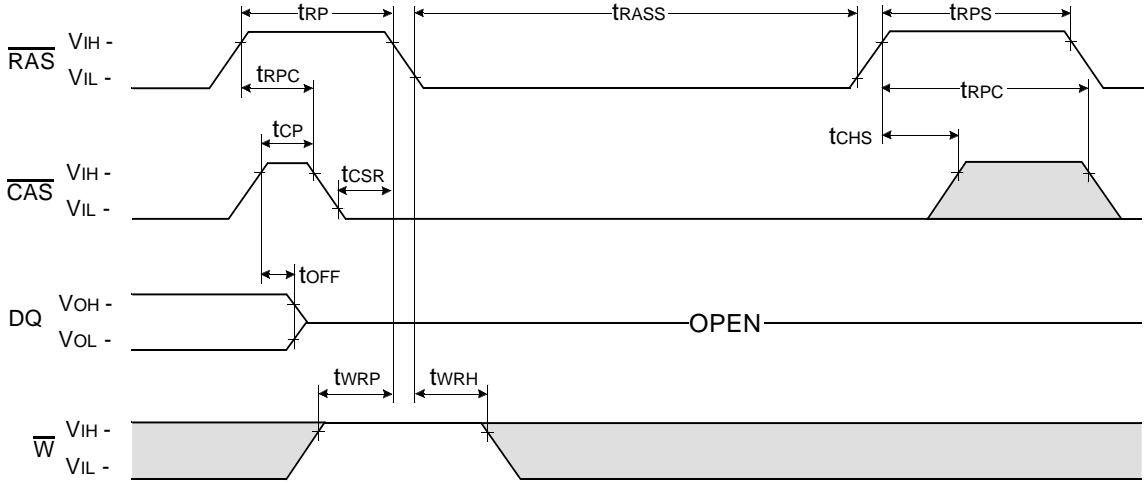


NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

DRAM MODULE

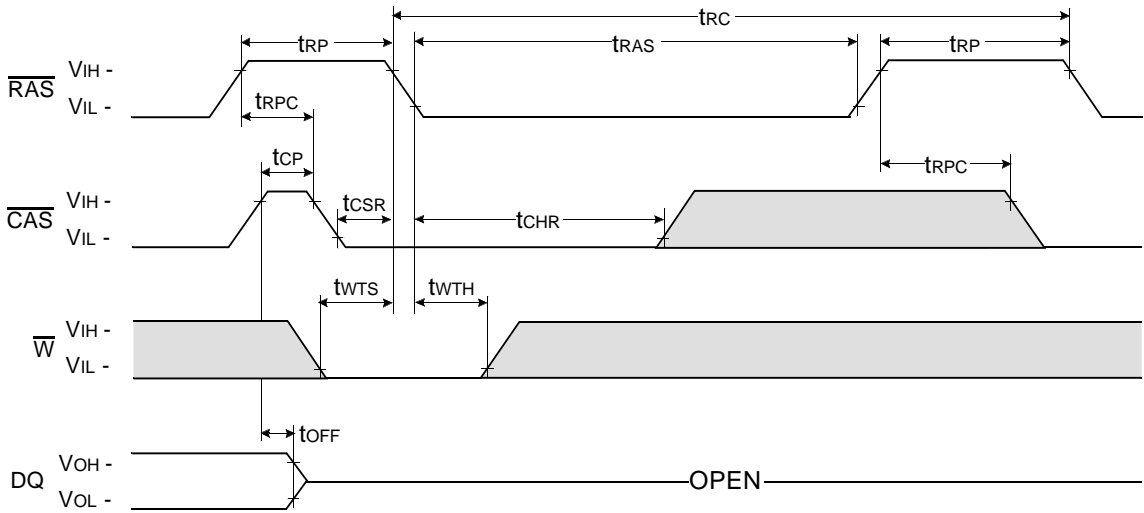
**CAS - BEFORE - RAS SELF REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



**TEST MODE IN CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



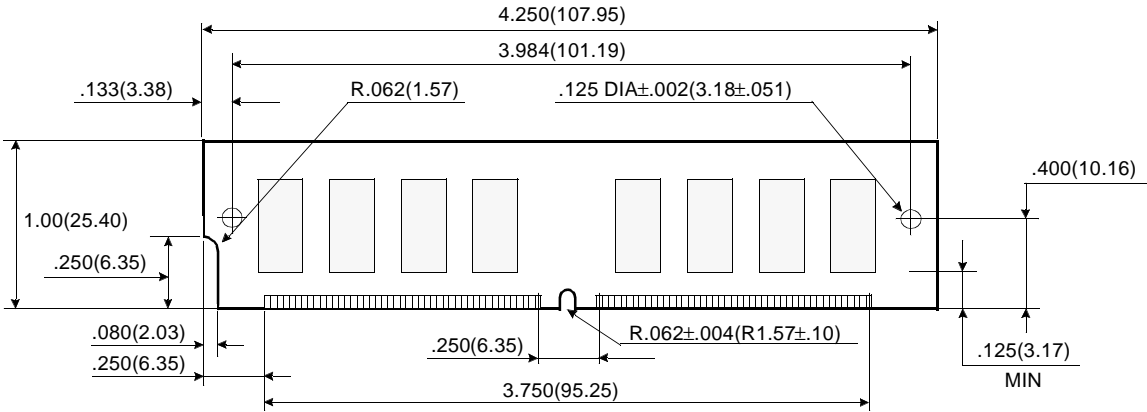
□ Don't care  
■ Undefined

**KMM5328000CK/CKG**  
**KMM5328100CK/CKG**

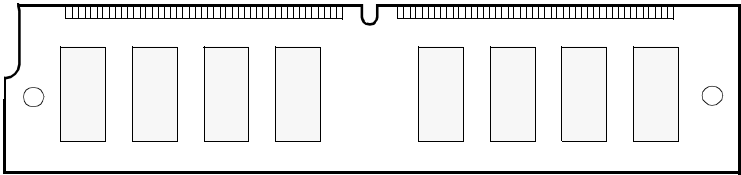
**DRAM MODULE**

**PACKAGE DIMENSIONS**

Units : Inches (millimeters)

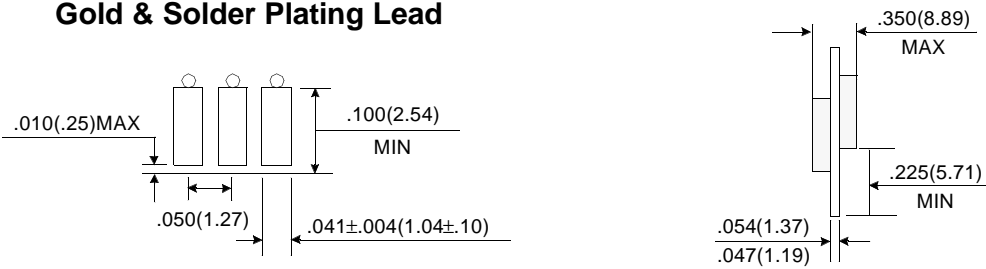


( Front view )



( Back view )

**Gold & Solder Plating Lead**



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device are 4Mx4 F/P DRAM, SOJ  
 DRAM Part No. : KMM5328000CK/CKG -- KM44C4000CK (300mil)  
 KMM5328100CK/CKG -- KM44C4100CK (300mil)

Revision History  
 Rev 0.0 : Aug. 1997

